UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,491	10/30/2003	Ross E. Johnson	ROC920030025US1	8050

30206 7590 03/22/2007

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
INGBERG, TODD D	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,491	JOHNSON, ROSS E.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/30/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 31 have been examined.

Claims 29 – 31 have been amended.

Information Disclosure Statement

1. The Information Disclosure Statement filed October 30,2003 has been considered.

Drawings

2. The Drawings filed October 30,2003 has been accepted.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 30 and 31 the rejected under 35 U.S.C. 101 had been overcome by amendment.

Contrary, to the statement on page 8 that dependent claims can not "undo" the statutory nature of a claim when is dependent because it inherits language from the parent claims. There are situations where dependent claims can in fact be rejected despite the parent claims. Under current Office policy on 101 this was one of the situations.

5. Claims 7 – 9 and 12 – 14 the rejected under 35 U.S.C. 101 has been overcome by explanation that the claim limitations are intended to mean a random testing of paths within the structure produced by the CFG. Previously, the Examiner had had interpreted the random ordering to change the behavior of the program which would result in non deterministic results.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Dean et al USPN # 6,070,009 issued May 30, 3000 and filed November 26, 1997.

Claim 1
Dean anticipates a method of ordering program code in a computer memory, the method comprising: selecting an ordering from among a plurality of orderings for a plurality of program code segments using a heuristic algorithm; and ordering the plurality of program code segments in a memory of a computer using the selected ordering. Dean, col 22, line 5 to line 55.

Claim 2
The method of claim 1, wherein the heuristic algorithm is configured to minimize cache misses in the computer. Dean, col 22, lines 5 – 54

Claim 3
The method of claim 1, wherein the heuristic algorithm comprises a simulated annealing algorithm. Dean, col 22, lines 5 – 34

Claim 4
The method of claim 3, wherein selecting the ordering using the heuristic algorithm includes testing a subset of the plurality of orderings. Dean, col 22, lines 9 - 17

Claim 5
The method of claim 4, wherein testing the subset of the plurality of orderings includes, for each ordering in the subset, calculating a cost for such ordering based upon cache miss rates for such ordering. As per claim 4 and claim 2.

Claim 6
The method of claim 5, wherein calculating the cost for each ordering comprises calculating a plurality of hits/reference values, misses/address values, and misses/entry values.
Col 21, lines 58 – 67 and col 22, lines 5 – 54.

Claim 7

The method of claim 5, wherein testing the subset of orderings includes randomly selecting a different ordering after testing an ordering from the subset of orderings. Dean, col 24, lines 1 – 10.

Claim 8
The method of claim 7, wherein randomly selecting the different ordering comprises swapping two program code segments in a previous ordering. Dean col 23 Line 7 to Col 24 line 10

Claim 9
The method of claim 8, wherein the program code segments each comprise a module, and wherein randomly selecting the different ordering further comprises constraining selection of the two program code segments to modules in the same replaceable unit destination. as per claims 7 and 8.

Claim 10
The method of claim 3, wherein selecting an ordering from among the plurality of orderings comprises testing a subset of orderings at each of a plurality of temperature values.
Dean, col 23, lines 7 to 24.

Claim 11
The method of claim 10, wherein selecting an ordering from among the plurality of orderings further comprises testing a subset of orderings at each temperature value.
As per claim 10.

Claim 12
The method of claim 11, wherein selecting an ordering from among the plurality of orderings further comprises accepting a change to an ordering if a calculated cost for such ordering is lower than that of a working ordering. Dean, col 24, line 30 – 46.

Claim 13
The method of claim 11, wherein selecting an ordering from among the plurality of orderings further comprises randomly accepting a change to an ordering even if the calculated cost for such ordering is not lower than that of the working ordering, Dean, col 24, lines 55 – 67.

Claim 14
The method of claim 11, wherein selecting an ordering from among the plurality of orderings further comprises prematurely halting the testing of orderings based upon a halt criterion.
Dean, Background of Invention – way to handle a stall.

Claim 15
The method of claim 1, wherein the program code segments each comprise a module from an operating system kernel.
Interpreted to be Call or Branch supported by OS and inherent in optimizing CFG (Dean, col 23, lines 55 – 65 – branch support).

Claim 16
The method of claim 15, wherein each module comprises a high use module, and wherein selecting the ordering from among a plurality of orderings comprises generating a high use module list. Dean, col 23 line 7 to col 24 line 23.

Claim 17
An apparatus, comprising: a processor; and first program code configured to be executed by the processor to optimize execution of second program code in a computer of the type including a multilevel memory architecture by using a heuristic algorithm to select an ordering from among a plurality of orderings for a plurality of program code segments in the second program code. As per claim 1.

Claim 18
The apparatus of claim 17, wherein the heuristic algorithm is configured to minimize cache misses in the computer. As per claim 2.

Claim 19
The apparatus of claim 17, wherein the heuristic algorithm comprises a simulated annealing algorithm. As per claim 3.

Claim 20
The apparatus of claim 19, wherein the first program code is configured to select the ordering using the heuristic algorithm by testing a subset of the plurality of orderings, and wherein the first program code is configured to test the subset of the plurality of orderings by, for each ordering in the subset, calculating a cost for such ordering based upon cache miss rates for such ordering. As per claims 4,2 and 6.

Claim 21
The apparatus of claim 20, wherein the first program code is configured to test the subset of orderings by randomly selecting a different ordering after testing an ordering from the subset of orderings. As per claim 7.

Claim 22
The apparatus of claim 21, wherein the first program code is configured to randomly select the different ordering by swapping two program code segments in a previous ordering. As per claim 8.

Claim 23
The apparatus of claim 22, wherein the program code segments each comprise a module, and wherein the first program code is configured to randomly select the different ordering by constraining selection of the two program code segments to modules in the same replaceable unit destination. As per claims 8 and 9.

Claim 24
The apparatus of claim 19, wherein the first program code is configured to select an ordering from among the plurality of orderings by testing a subset of orderings at each of a plurality of temperature values, and testing a subset of orderings at each temperature value. As per claims 8,9 and 10.

Claim 25
The apparatus of claim 24, wherein the first program code is configured to select an ordering from among the plurality of orderings by accepting a change to an ordering if a calculated cost for such ordering is lower than that of a working ordering. As per claim 12.

Claim 26
The apparatus of claim 25, wherein the first program code is configured to select an ordering from among the plurality of orderings by randomly accepting a change to an ordering even if the calculated cost for such ordering is not lower than that of the working ordering. As per claim 13.

Claim 27
The apparatus of claim 17, wherein the first program code is configured to select an ordering from among the plurality of orderings by prematurely halting the testing of orderings based upon a halt criterion. As per claim 14.

Claim 28
The apparatus of claim 17, wherein the program code segments each comprise a module from an operating system kernel.
Interpreted to be Call or Branch supported by OS and inherent in optimizing CFG (Dean, col 23, lines 55 – 65 – branch support).

Claim 29
The apparatus of claim 28, wherein each module comprises a high use module, and wherein the first program code is configured to select the ordering from among a plurality of orderings by generating a high use module list. (Dean, col 23, lines 14 – 24).

Claim 30
Dean anticipates a program product, comprising: first program code configured to optimize execution (Dean, Abstract – Abstract of Invention) of second program code in a computer of the type including a multi-level memory architecture (Dean, Figure 1, #112, 113, 121, 122 ,123) by using a heuristic algorithm to select an ordering from among a plurality of orderings (Dean, col 24, lines 1 – 10) for a plurality of program code segments in the second program code (Dean, Abstract, last sentence – counting is a heuristic); and a physical computer readable medium bearing the first program code.

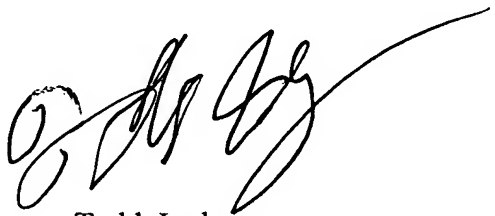
Claim 31
The program product of claim 30, wherein the computer readable medium includes a recordable medium. Dean, Figure 1.

Correspondence Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Todd Ingberg
Primary Examiner
Art Unit 2193

TI